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Justina S. Townsend

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	Group Art Unit: 2634
Ronald M. Hickling	:	Examiner: Young T. Tse
Title: **Direct Conversion Delta-Sigma Receiver**	:	
Serial No.: 09/241,994	:	
Filed: February 2, 1999	:	

Commissioner for Patents
Washington, D.C. 20231

RESPONSE TO OFFICE ACTION DATED JULY 16, 2001

Sir:

In response to the Office Action dated July 16, 2001, please amend the above-identified application as follows:

In the specification please rewrite the following paragraphs as indicated below:

Pages 2, lines 19 – 25:

The output from the amplifier 26 is input into a sample and hold circuit 28. The sample and hold circuit 28 is clocked by a first clock having a frequency f_1. The output of the sample and hold circuit 28 comprises a series of copies of the modulated signal centered about multiples of the clock frequency f_1. The output of the sample and hold circuit 28 is coupled to an oversampling delta-sigma converter 30. The delta-sigma converter 30 receives a second clock having a frequency, f_2, which is an integer multiple of the frequency f_1. In this way, the delta-sigma converter loop 30 oversamples the output signal provided by the sample and hold circuit 28; thus, after decimation filtering providing a quantized representation of the modulated signal.

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